- **8-Bit Resolution**
- **±0.2% Linearity**
- **Maximum Conversion Rate**
  30 MHz Typ
  20 MHz Min
- **Analog Output Voltage Range**
  V_{DD} to V_{DD} −1 V

- **TTL Digital Input Voltage**
- **5-V Single Power-Supply Operation**
- **Low Power Consumption . . . 80 mW Typ**
- **Interchangeable With Fujitsu MB40778**

description

The TLC5602x devices are low-power, ultra-high-speed video, digital-to-analog converters that use the LinEPIC™ 1-μm CMOS process. The TLC5602x converts digital signals to analog signals at a sampling rate of dc to 20 MHz. Because of high-speed operation, the TLC5602x devices are suitable for digital video applications such as digital television, video processing with a computer, and radar-signal processing.

The TLC5602C is characterized for operation from 0°C to 70°C. The TLC5602M is characterized over the full military temperature range of −55°C to 125°C.

N PACKAGE
(TOP VIEW)

DGTL GND	1	18	D0 (LSB)
DGTL V_{DD}	2	17	D1
COMP	3	16	D2
REF	4	15	D3
ANLG V_{DD1}	5	14	D4
A OUT	6	13	D5
ANLG V_{DD2}	7	12	D6
DGTL V_{DD}	8	11	D7 (MSB)
ANLG GND	9	10	CLK

DW PACKAGE
(TOP VIEW)

DGTL GND	1	20	NC
DGTL V_{DD}	2	19	D0 (LSB)
COMP	3	18	D1
REF	4	17	D2
ANLG V_{DD1}	5	16	D3
A OUT	6	15	D4
NC	7	14	D5
ANLG V_{DD2}	8	13	D6
DGTL V_{DD}	9	12	D7 (MSB)
ANLG GND	10	11	CLK

J PACKAGE
(TOP VIEW)

NC	1	20	NC
DGTL GND	2	19	D0 (LSB)
DGTL V_{DD}	3	18	D1
COMP	4	17	D2
REF	5	16	D3
ANLG V_{DD1}	6	15	D4
A OUT	7	14	D5
ANLG V_{DD2}	8	13	D6
DGTL V_{DD}	9	12	D7 (MSB)
ANLG GND	10	11	CLK

FK PACKAGE
(TOP VIEW)

Top pins (left to right): DGTL V_{DD} (3), DGTL GND (2), NC (1), NC (20), D0 (LSB) (19)

Left pins (top to bottom): COMP (4), REF (5), ANLG V_{DD1} (6), A OUT (7), ANLG V_{DD2} (8)

Right pins (top to bottom): D1 (18), D2 (17), D3 (16), D4 (15), D5 (14)

Bottom pins (left to right): DGTL V_{DD} (9), ANLG GND (10), CLK (11), D7 (MSB) (12), D6 (13)

NC—No internal connection

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TEXAS INSTRUMENTS

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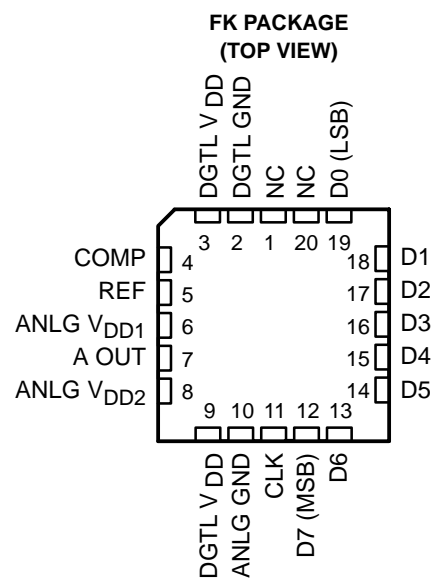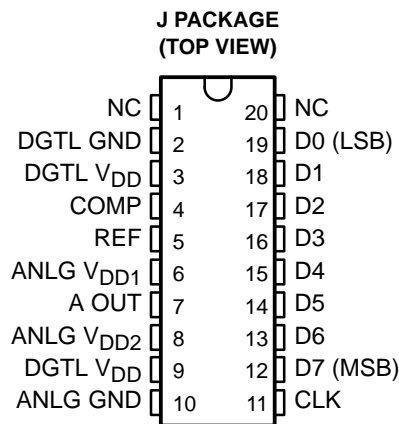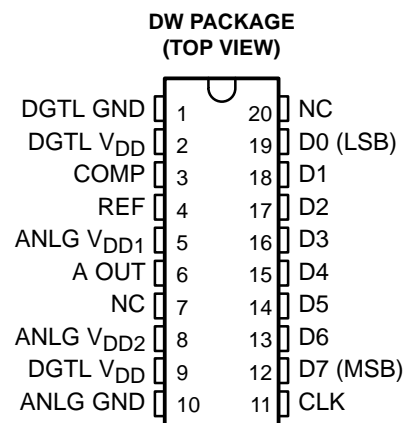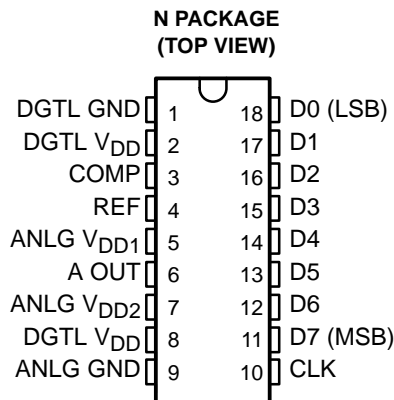
TLC5602C, TLC5602M
VIDEO 8-BIT DIGITAL-TO-ANALOG CONVERTERS

AVAILABLE OPTIONS

	PACKAGE			
T_A	WIDE-BODY SMALL OUTLINE (DW)	CERAMIC CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLC5602CDW			TLC5602CN
−55°C to 125°C		TLC5602MFK	TLC5602MJ	

functional block diagram
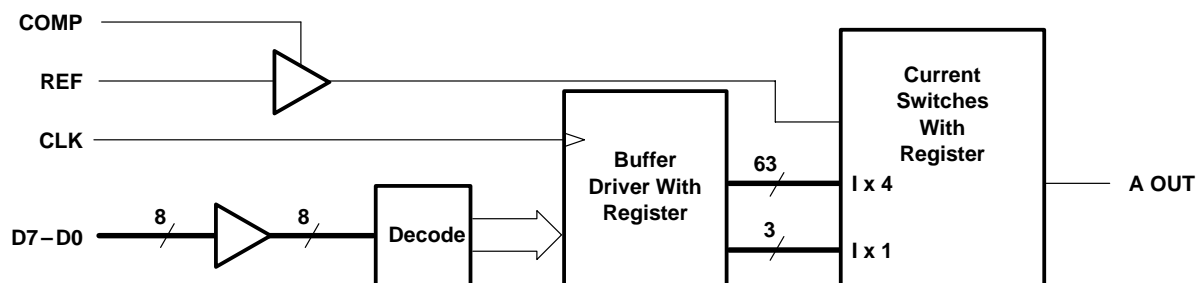
FUNCTION TABLE

STEP	DIGITAL INPUTS								OUTPUT VOLTAGE†
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.980 V
1	L	L	L	L	L	L	L	H	3.984 V
|				|					|
127	L	H	H	H	H	H	H	H	4.488 V
128	H	L	L	L	L	L	L	L	4.492 V
129	H	L	L	L	L	L	L	H	4.496 V
|				|					|
254	H	H	H	H	H	H	H	L	4.996 V
255	H	H	H	H	H	H	H	H	5.000 V

† V_{DD} = 5 V and V_{ref} = 4.02 V

![Texas Instruments logo] **TEXAS INSTRUMENTS**

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schematics of equivalent input and output

EQUIVALENT OF EACH DIGITAL INPUT	EQUIVALENT OF ANALOG OUTPUT
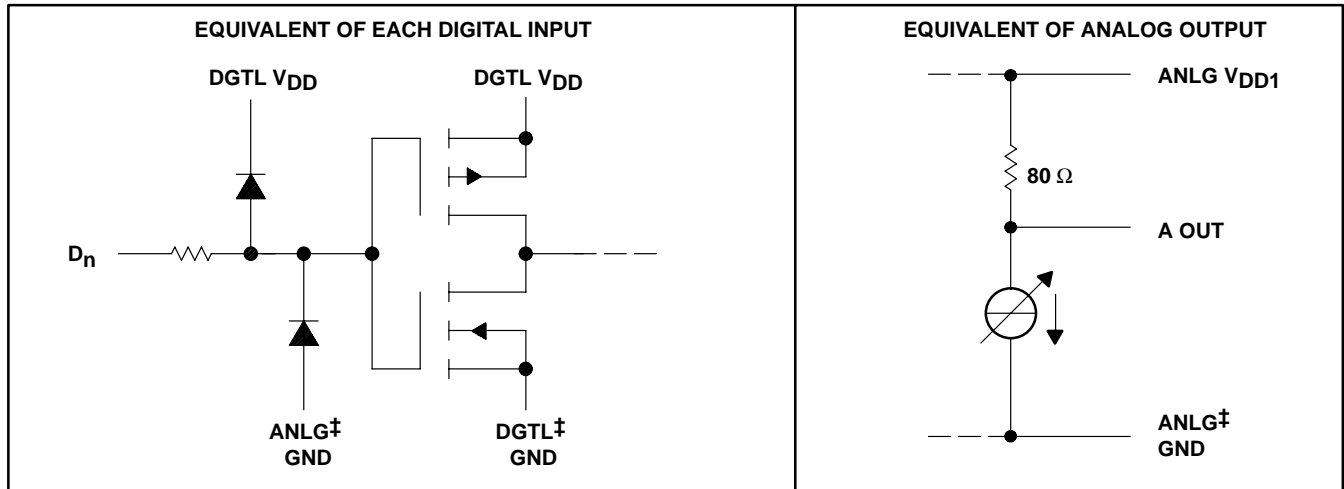
‡ ANLG GND and DGTL GND do not connect internally and should be tied together as close to the device terminals as possible.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, ANLG V_{DD}, DGTL V_{DD} .... −0.5 V to 7 V
Digital input voltage range, V_I .... −0.5 V to 7 V
Analog reference voltage range, V_{ref} .... $V_{DD} − 1.7$ V to $V_{DD} + 0.5$ V
Operating free-air temperature range, T_A: TLC5602C .... 0°C to 70°C
TLC5602M .... −55°C to 125°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	V
Analog reference voltage, V_{ref}		3.8	4	4.2	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Pulse duration, CLK high or low, t_w		25			ns
Setup time, data before CLK↑, t_{su}		16.5			ns
Hold time, data after CLK↑, t_h		12.5			ns
Phase compensation capacitance, C_{comp} (see Note 1)		1			µF
Load resistance, R_L		75			Ω
Operating free-air temperature, T_A	TLC5602C	0		70	°C
	TLC5602M	−55		125	

NOTE 1: The phase compensation capacitor should be connected between COMP and ANLG GND.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current	Digital inputs	$V_I = 5$ V			±1	µA
I_{IL}	Low-level input current		$V_I = 0$ V			±1	µA
I_{ref}	Input reference current		$V_{ref} = 4$ V			10	µA
V_{FS}	Full-scale analog output voltage		$V_{DD} = 5$ V, $\quad V_{ref} = 4.02$ V		$V_{DD}-15$	V_{DD}	$V_{DD}+15$	mV
V_{ZS}	Zero-scale analog output voltage		$V_{DD} = 5$ V, $\quad V_{ref} = 4.02$ V, T_A = full range§	TLC5602C	3.919	3.98	4.042	V
				TLC5602M	3.919	3.98	4.042	
				TLC5602M	3.919	3.98	4.062	
r_o	Output resistance		$T_A = 25°C$	TLC5602C	60	80	120	Ω
			T_A = full range§	TLC5602M				
C_i	Input capacitance		$f_{clock} = 1$ MHz, $\quad T_A = 25°C$			15		pF
I_{DD}	Supply current		$f_{clock} = 20$ MHz, $\quad V_{ref} = V_{DD}-0.95$ V			16	25	mA

‡ All typical values are at $V_{DD} = 5$ V and $T_A = 25°C$.
§ Full range for the TLC5602C is 0°C to 70°C, and full range for the TLC5602M is −55°C to 125°C.

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$E_{L(adj)}$	Linearity error, best-straight-line	T_A = full range‡	TLC5602C			$\pm0.2\%$	
		$T_A = 25°C$	TLC5602M			$\pm0.2\%$	
		T_A = full range‡				$\pm0.4\%$	
E_L	Linearity error, end point				$\pm0.15\%$		
E_D	Linearity error, differential					$\pm0.2\%$	
G_{diff}	Differential gain	NTSC 40-IRE modulated ramp, $f_{clock} = 14.3$ MHz, $Z_L \geq 75$ kΩ			0.7%		
f_{diff}	Differential phase				0.4°		
t_{pd}	Propagation delay time, CLK to analog output	$C_L = 10$ pF			25		ns
t_s	Settling time to within 1/2 LSB	$C_L = 10$ pF			30		ns

† All typical values are at $V_{DD} = 5$ V and $T_A = 25°C$.
‡ Full range for the TLC5602C is 0°C to 70°C, and full range for the TLC5602M is −55°C to 125°C.
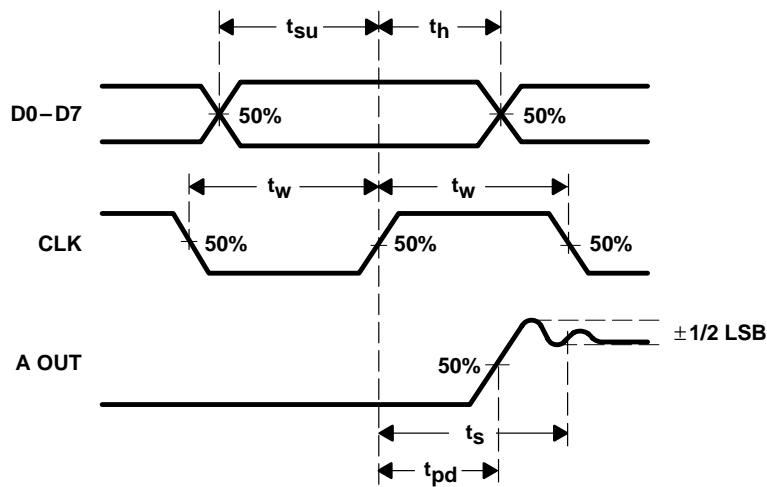
PARAMETER MEASUREMENT INFORMATION

Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS

IDEAL CONVERSION CHARACTERISTICS

Figure 2

BEST-STRAIGHT-LINE LINEARITY ERROR
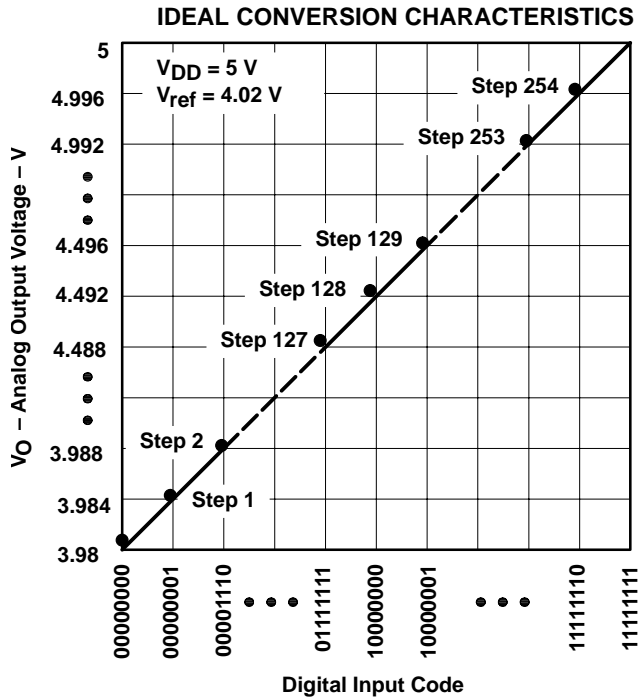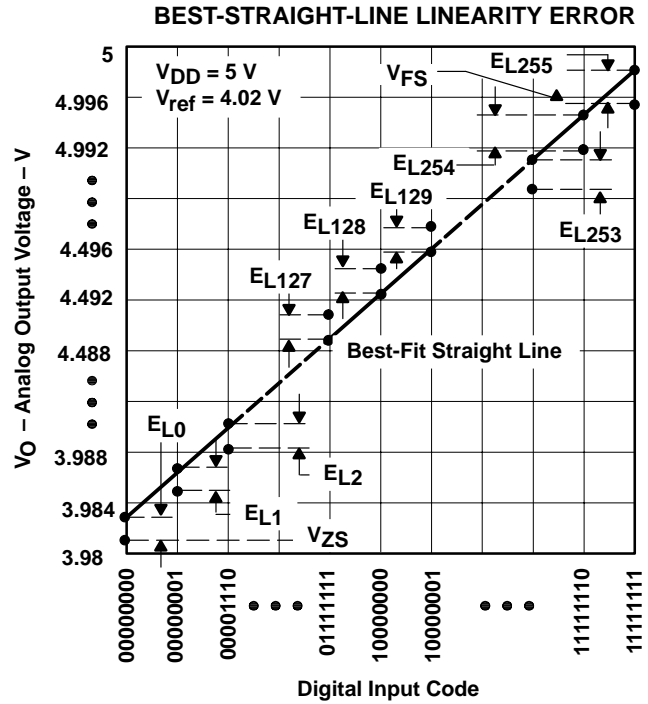
Figure 3

ZERO-SCALE OUTPUT VOLTAGE
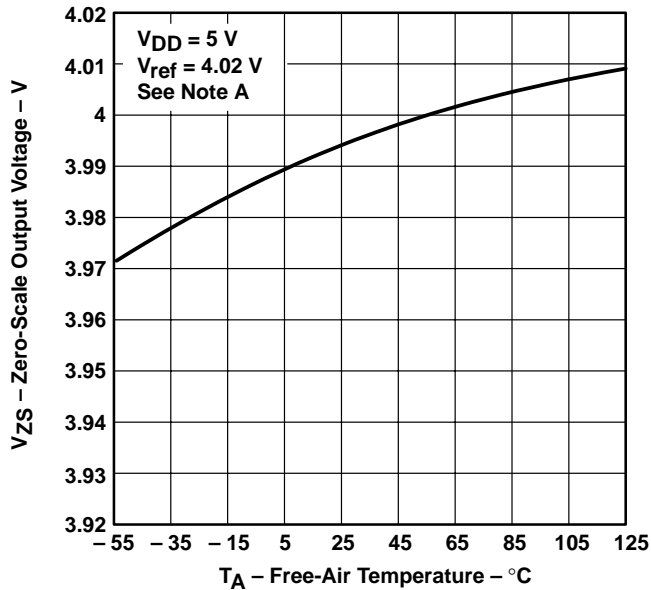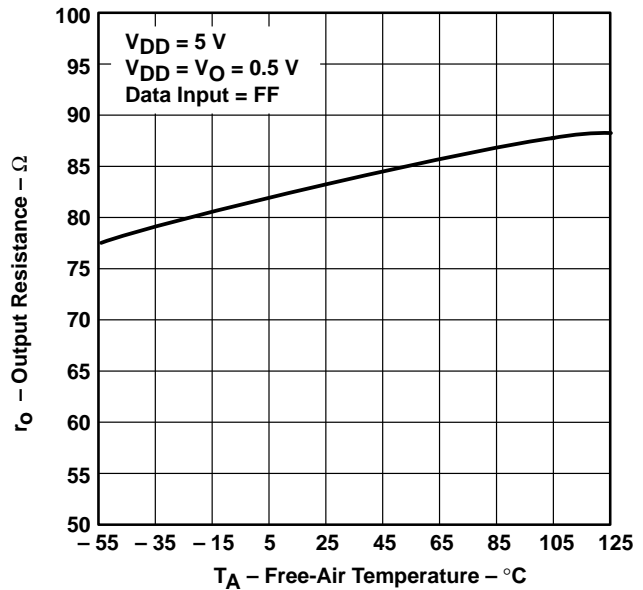### vs
FREE-AIR TEMPERATURE
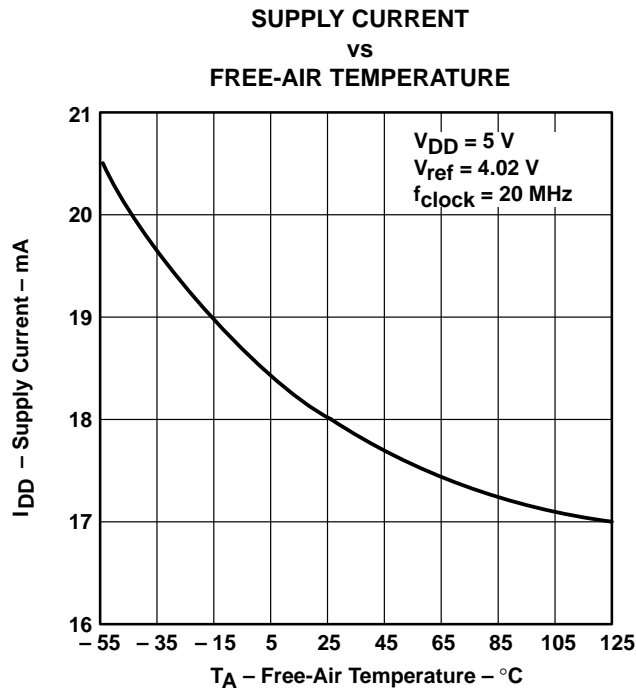

NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

Figure 4

OUTPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

Figure 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

$V_{DD} = 5$ V
$V_{ref} = 4.02$ V
$f_{clock} = 20$ MHz

Figure 6

ZERO-SCALE OUTPUT VOLTAGE
vs
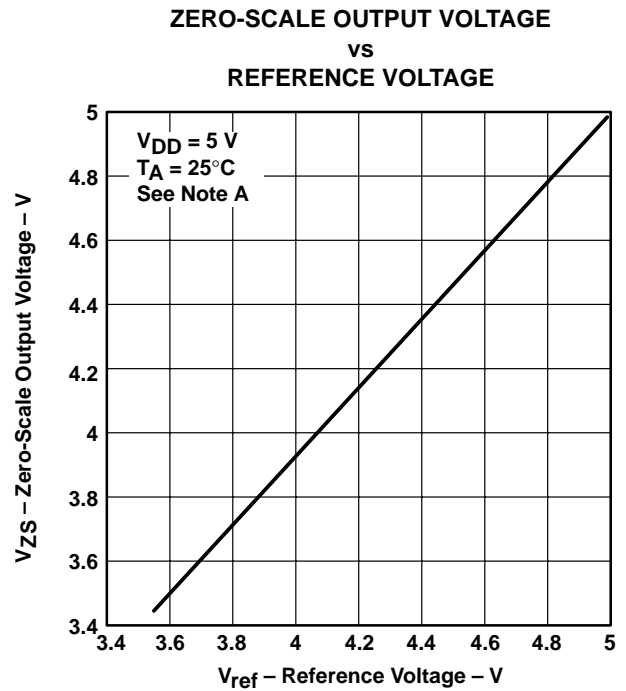**REFERENCE VOLTAGE**

$V_{DD} = 5$ V
$T_A = 25°C$
See Note A

NOTE A: V_{ref} is relative to ANLG GND. V_{DD} is the voltage between ANLG V_{DD} and DGTL V_{DD} tied together and ANLG GND and DGTL GND tied together.

Figure 7

APPLICATION INFORMATION

The following design recommendations benefit the TLC5602 user:

- Physically separate and shield external analog and digital circuitry as much as possible to reduce system noise.

- Use RF breadboarding or RF printed-circuit-board (PCB) techniques throughout the evaluation and production process.

- Since ANLG GND and DGTL GND are not connected internally, these terminals need to be connected externally. With breadboards, these ground lines should connect to the power-supply ground through separate leads with proper supply bypassing. A good method is to use a separate twisted pair for the analog and digital supply lines to minimize noise pickup.

  Use wide ground leads or a ground plane on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.

- ANLG V_{DD} and DGTL V_{DD} are also separated internally, so they must connect externally. These external PCB leads should also be made as wide as possible. Place a ferrite bead or equivalent inductance in series with ANLG V_{DD} and the decoupling capacitor as close to the device terminals as possible before the ANLG V_{DD} and DGTL V_{DD} leads are connected together on the board.

- Decouple ANLG V_{DD} to ANLG GND and DGTL V_{DD} to DGTL GND with a 1-μF and 0.01-μF capacitor, respectively, as close as possible to the appropriate device terminals. A ceramic chip capacitor is recommended for the 0.01-μF capacitor.

- Connect the phase compensation capacitor between COMP and ANLG GND with as short a lead-in as possible.

- The no-connection (NC) terminals on the small-outline package should be connected to ANLG GND.

- Shield ANLG V_{DD}, ANLG GND, and A OUT from the high-frequency terminals CLK and D7–D0. Place ANLG GND traces on both sides of the A OUT trace on the PCB.

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