Application Note

BIT3193

High Performance PWM Controller

Version 1.0

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BIT3193 Application note

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Abstract

BiTEK new developed BIT3193 general purpose PWM controller with a kind of two output signals with 180 degree out of phase. A built-in low frequency PWM generator makes the design job easy especially when you need it in the application circuit. Latched-off functions, which are also built-in, make BIT3193 more reliable in system protection. A Built-in soft-start function simplifies the peripheral circuit design and reduces inrush current when the system is starting-up. The highly integrated design of BIT3193 get the both advantages of high performance and low price.

1. Introduction

General purposed PWM controllers developed in many specified application like switching power supply design are popular especially when designed for various topologies. They can increase the efficiency more comparing to the traditional Fly-back converters and Forward converters.

For various topologies of converter design, the output voltage feeds a voltage signal into the input of an error amplifier for comparing to the reference voltage, and then the error amplifier delivers an error signal by a compensation circuit. This error signal is modulated as PWM signal by comparing with a triangular wave. There are some logic timing circuits to separate the phases of this PWM signal to have a dual-PWM-output to drive power switches of used power circuit. Beside the basic functions of feedback control in different converter design, some specific applications such as to use a DC/PWM transfer circuit without feedback are also popular. Such signal can be used as an indication signal or simple ON/OFF control to other systems.

To avoid inrush current when the switching power been turned on, normally it needs a soft-start circuit. The built-in soft-start function can reduce the number and rating of external components and increases the system reliability. This specific function latches the designed system that can also avoid the more serious problems. A Clamped circuit design provides a fast response loop to reduce the output voltage when there is a high output voltage occurred in the initial stage. The Low power consumption by adopting CMOS process for controller provides the system higher efficiency.

2. BIT3193 functional description

Fig. 1 shows a block diagram of BIT3193. All of its detailed internal block diagrams show in following sections.

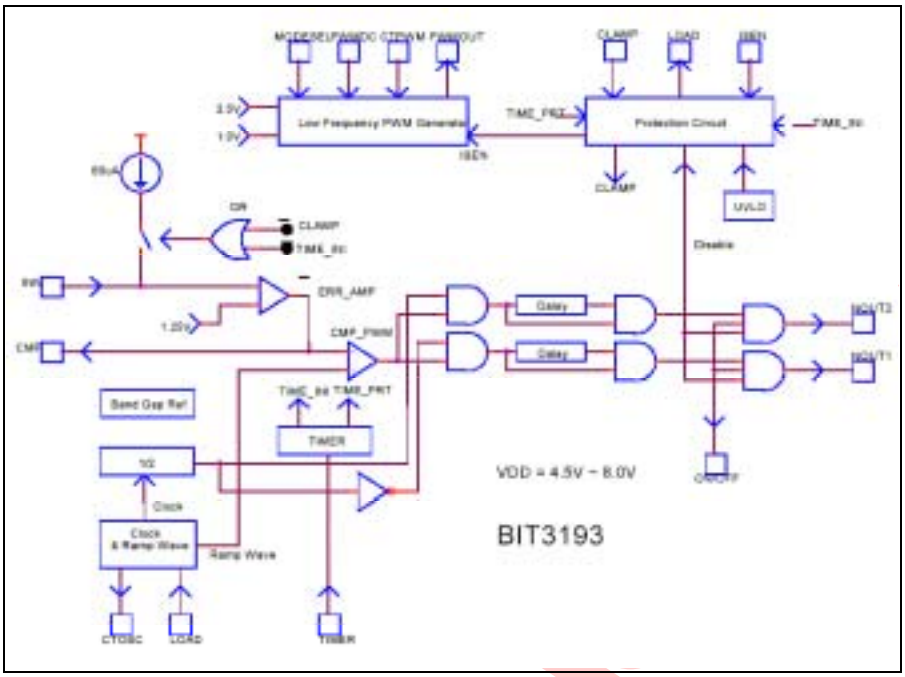

Fig. 1 BIT3193 block diagram

2.1. INN and CMP

The INN pin and the CMP pin are the input and output of the error amplifier in BIT3193, which is shown as Fig. 2. The PWM signal is generated when a triangular wave and a DC voltage feed into CMP_PWM. The error amplifier has the job of compensation for the whole system in a close-loop design by accomplishing with a RC-network. The triangular wave is generated when a capacitor connected in CTOSC pin. About the basic operation of error amplifier, the INN pin is worked to receive the feedback signal then compare it with an internal 1.25V reference voltage in the error amplifier (ERR_AMP). The error amplifier works as both a comparator and a compensator when a RC-network connected between its output pin and INN pin. The tolerance of 1.25V reference voltage in BIT3193 is designed as ±3%.

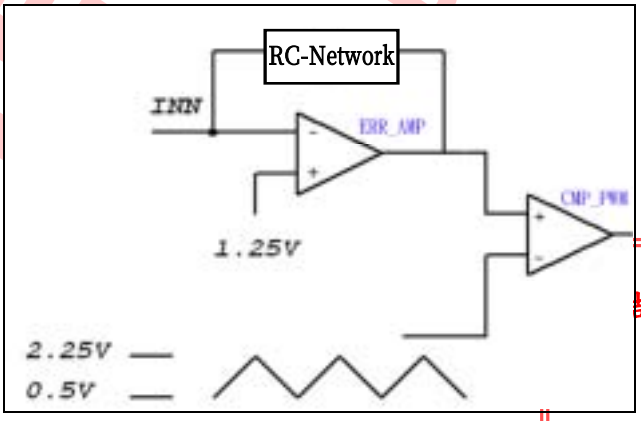

Fig. 2 Error amplifier and modulation

2.2. Clock and ramp wave generator

A capacitor is connected in CTOSC pin, which can produce a triangular wave; the frequency of this wave is also called the oscillation frequency, shown as Fig. 3. Comparing with 0.5V and 2.25V, the two current sources charged and discharged then generate the necessary triangular wave. The relationship of frequency and capacitor value is shown as Fig. 4. In addition, BIT3193 is a two output signals with 180 degree out of phase and its triangular frequency is double of its output frequency.

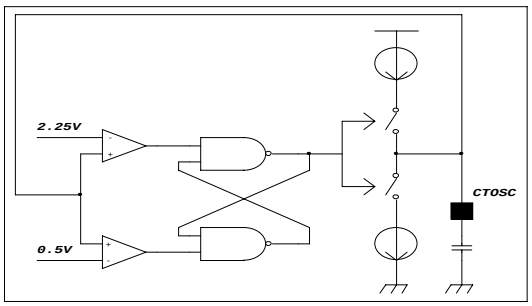

Fig. 3 The schematic of ramp wave generator

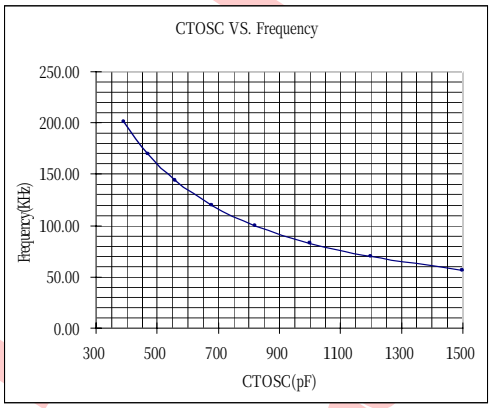

Fig. 4 The relationship of CTOSC and frequency

The generated frequency can be referred as following equation:

$$F_{HFPWM} = \frac{K_{HF}}{C_{CTOSC}},\ K_{HF} = 8.2e-5$$

If the required frequency is 50kHz, the selected triangular wave frequency is 100kHz, therefore we can know:

$$100kHz = \frac{8.2e-5}{C_{CTOSC}}$$

And choose a 820pF capacitor and connect it to CTOSC pin.

In addition, considering about temperature factor and the tolerance of capacitor, to choose the NPO type with ±5% tolerance so as to meet the requirement,±8% design specification, because of the ±3% frequency tolerance of BIT3193. For a 50 KHz frequency design, the maximum tolerance of ±8% equals ±4KHz.

2.3. LOAD Resistor vs. CTOSC Frequency

BIT3193 supports the higher start-up frequency when a resistor connected to its LOAD pin, shown as Fig 5. The function of LOAD pin is related to ISEN pin. When the voltage of ISEN pin is lower than 1.3V, the internal switch (connected to LOAD pin) is “closed” that makes BIT3193 generate a higher start-up frequency. When the voltage of ISEN pin is higher than 1.3V, the internal switch connected is “opened” that makes BIT3193 generate a normal operation frequency. The relationship of LOAD resistor and CTOSC frequency deviation is shown as Fig. 6.

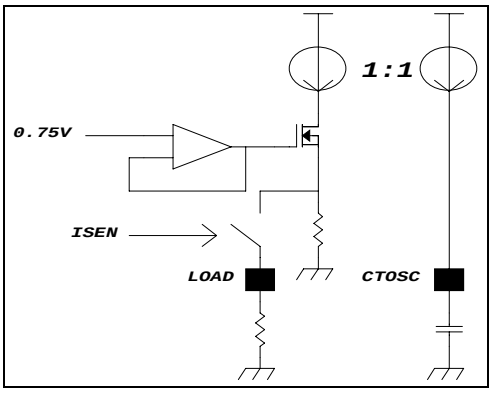

Fig. 5 Connected a resistor in LOAD pin

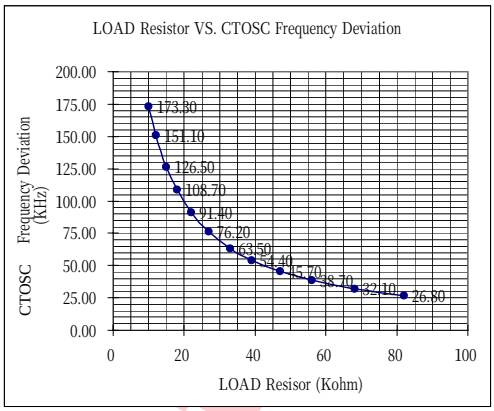

Fig. 6 LOAD resistor vs. CTOSC frequency deviation

The equation of deviation is shown as following equation:

$$\Delta Fn = \frac{\Delta F100_{KHz} \times F_n}{100KHz}$$

When CTOSC is in 100KHz and the start-up frequency is 140KHz, ΔFn will be 40KHz and the resistor connected to LOAD will be 51KΩ.

2.4. Timing diagram

The output PWM signal is accomplished by comparing the ramp wave and the output of error amplifier (CMP_PWM OUT). The ramp wave is generated in CTOSC pin when a capacitor is connected here; its frequency is determined by the capacitor. The Delay elements and AND logics feed the PWM signal of CMP_PWM into NOUT1 and NOU2. To avoid a short circuit happened between NOUT1 and NOUT2, the delay time is needed and must be enough.

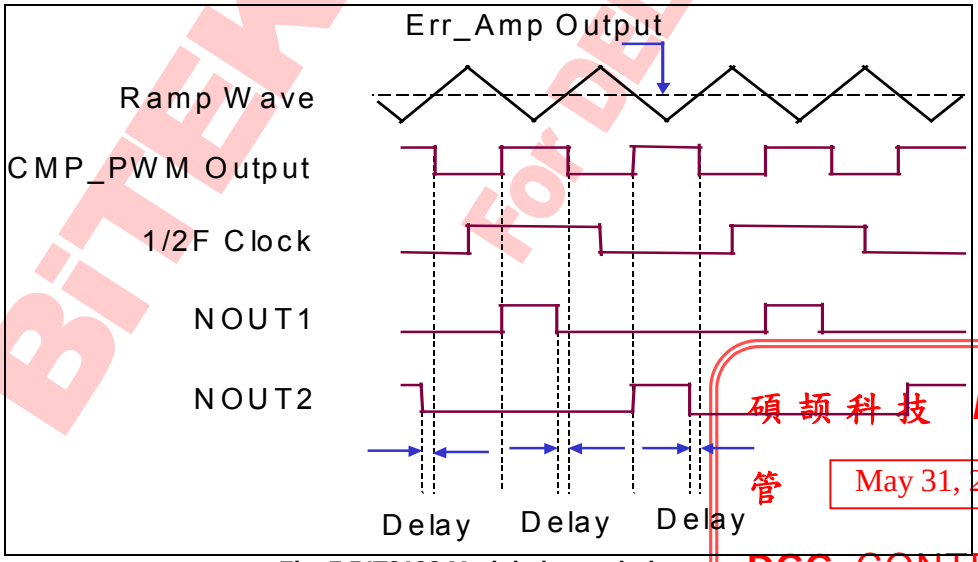

Fig. 7 BIT3193 Modulation technique

2.5. ISEN and Timer

The TIMER pin is charged by an internal current source when an external capacitor is connected to this pin. The timing chart is shown as Fig. 8. Firstly, the ON/OFF input voltage of BIT3193 is higher than 1V, the voltage of TIMER pin is lower than 0.5V and there is no signal input on ISEN pin, the period in above conditions is called "Turn on delay time". During the "Turn on delay time" there is no signal for NOUT output. Secondly, TIMER pin increases its charged voltage to make NOUT enable until it is in 2.5V. Thirdly, because there is no signal fed into ISEN, BIT3193 will count 32 cycles based on CTPWM cycle time then shut itself down when the voltage of TIMER pin is higher than 2.5V.

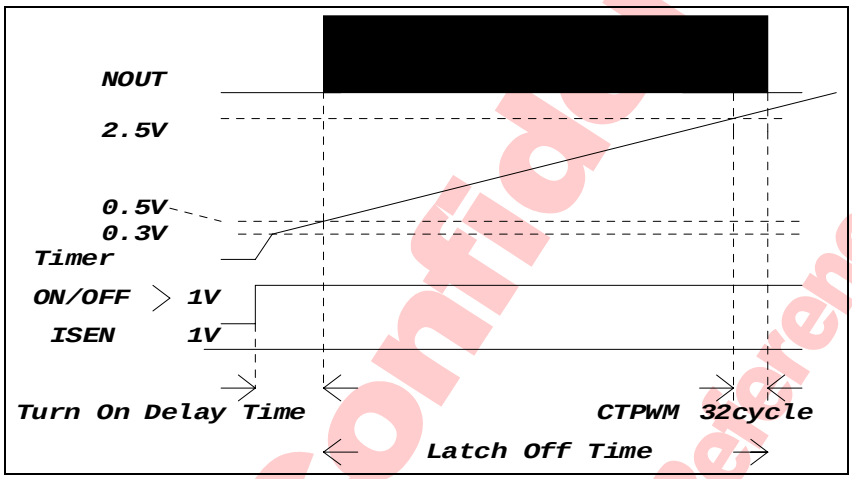

Fig. 8 ISEN and TIMER

Fig. 9 is another condition when the voltage of TIMER pin is higher than 2.5V, NOUT has normal output and ISEN detects a signal, which is higher than 1.3V in its first state. The second state is that ISEN detects nothing and becomes low. This condition will not shut BI3193 down immediately because it assumes this condition maybe caused by noise, then the internal counter of BIT3193 begins to count 32 cycles. If the voltage of ISEN pin is still lower than 1.3V after 32 cycles then BIT3193 will shut itself down.

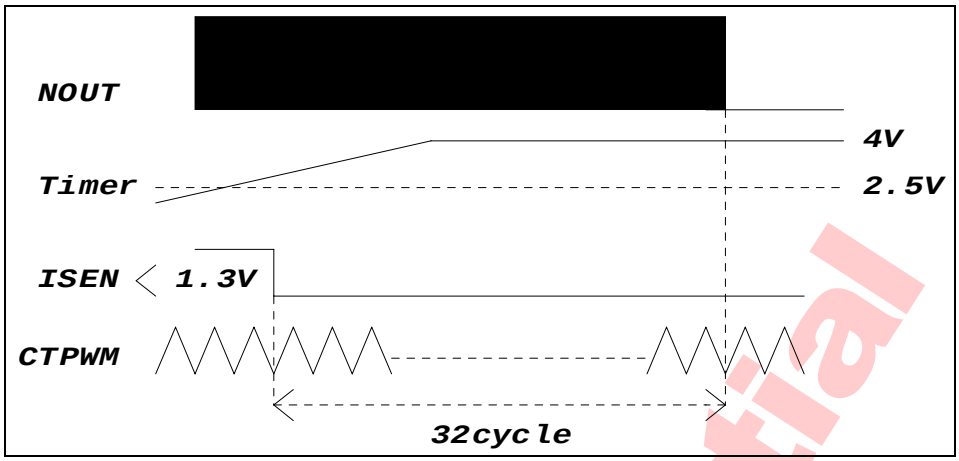

Fig. 9 Delay time of ISEN

The realized circuit is shown as Fig. 10. The two comparators compare TIMER pin voltage and ISEN pin voltage to 2.5V and 1.3V respectively. After delayed 32 cycles, the Latch Circuit may decide to disable BIT3193.

Besides, BIT3193 offers ON/OFF pin to turn on/off itself when there is an input voltage higher than 1V, shown as Fig. 10. There is a built-in 80KΩ resistor connected to ground in ON/OFF pin and engineers need to pay attention more about the load effect of it. When IC supplied voltage is 5V and a 200KΩ resistor connects to ON/OFF pin, an about 1.42V voltage in this pin may turn on BIT3193. Such kind of turn-on/off circuit needs a paralleled capacitor connected here to avoid the noise interference in this pin. When start up BIT3193 by turning on its ON/OFF pin, all of IC's internal functions will be reset to ensure all the parameters in initial states. These initial states are built when the voltage of TIMER pin is between 0V and 0.3V.

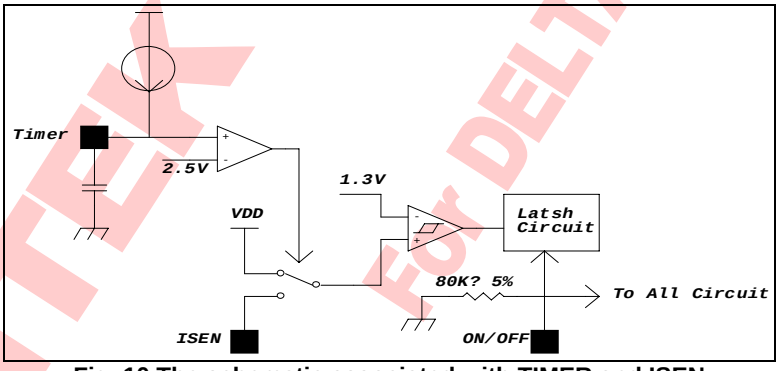

Fig. 10 The schematic associated with TIMER and ISEN

2.6. Low frequency PWMOUT

The realized circuit of low frequency PWMOUT with polarity selection is shown as Fig. 11. The maximum voltage and minimum voltage of triangular wave are 2.5V and 0.5V respectively. The frequency of triangular wave is controlled by the capacitor connected to CTPWM pin and the duty cycle of PWMOUT is controlled by PWMDC voltage level. Finally, the signal voltage level of MODE controls the polarity of PWMOUT.

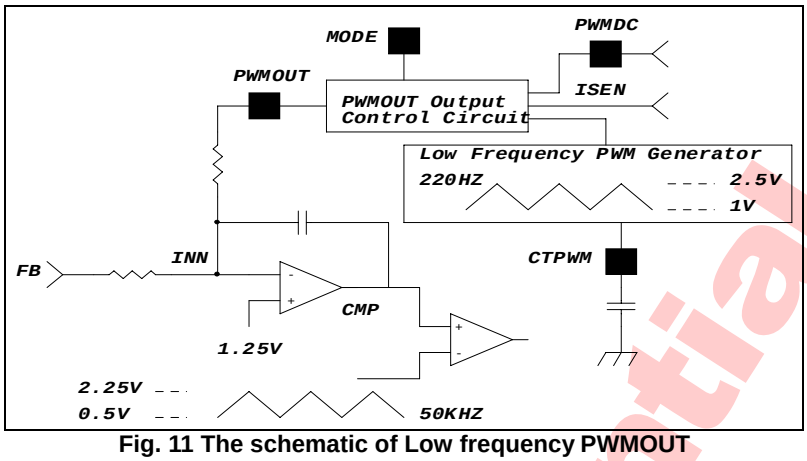

Fig. 11 The schematic of Low frequency PWMOUT

The PWMOUT pin generates a low frequency PWM signal when the level of ISEN is higher than 1.3V, shown as Fig. 12. The duty cycle of PWMOUT is proportional to PWMDC when MODE pin is connected to ground. In the other side, the duty cycle of PWMOUT is inverse proportional to PWMDC when MODE pin is connected to a logic high level (e. g. IC_VDD). When a 0.022uF capacitor is selected to connect to CTPWM pin that can produce the frequency about 220Hz. To choose X7R type of capacitors can avoid frequency from drafted when environmental temperature is changed.

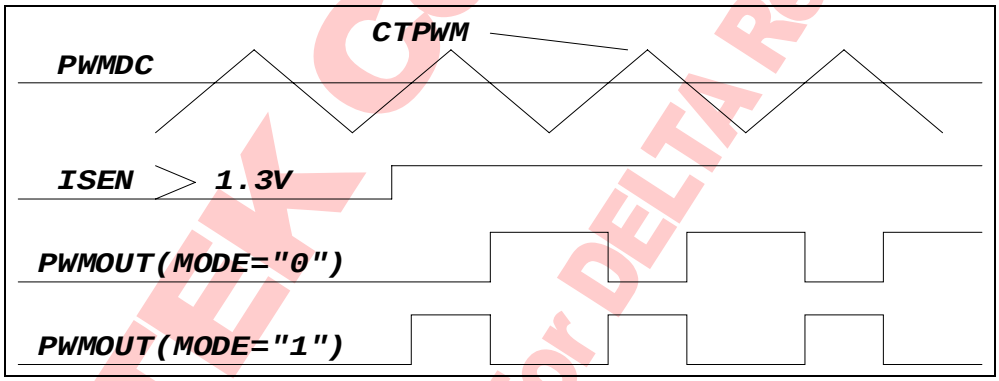

Fig. 12 MODE vs. PWMOUT

For the proportional relationship of PWMOUT duty cycle and PWMDC, when MODE is selected to logic “0” then PWMOUT has the maximum duty cycle limitation of 92%, shown as Fig. 13.

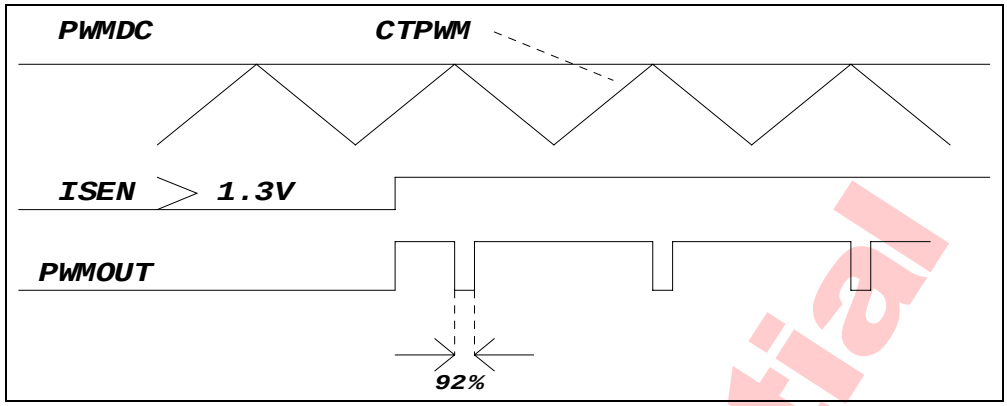

Fig. 13 PWMOUT maximum duty cycle limitation

2.7. BIT3193 initial status

Shown in Table 1 are initial states of BIT3193 when it is powered on. During the initial state, there will be a 60uA current flows into INN pin, the error amplifier input in BIT3193, to make the output of error amplifier as the low level. Output pins of NOUT1 and NOUT2 are in the same level with ground and two frequency generators, high triangular wave and low frequency triangular wave, have normal oscillation signals.

Table 1 BIT3193 initial state

Pin Number	Pin Name	Status
1	INN	Force to VDD (With ~ 60uA current source)
4	CTOSC	Normally run
8	NOUT1	Forced to GND
9	NOUT2	Forced to GND
11	PWMOUT	Floating
12	CTPWM	Normally run

2.8. Over voltage clamping

The internal circuit of CLAMP pin in BIT3193 is designed by comparing with 2V, shown as Fig. 14. When a signal voltage higher than 2Vwhich feeds to CLAMP pin then the internal switch will be turned on to let the 60uA current flow to INN pin to increase the potential level of INN pin and reduces the potential level of CMP, hence the NOUT duty cycle will be reduced.

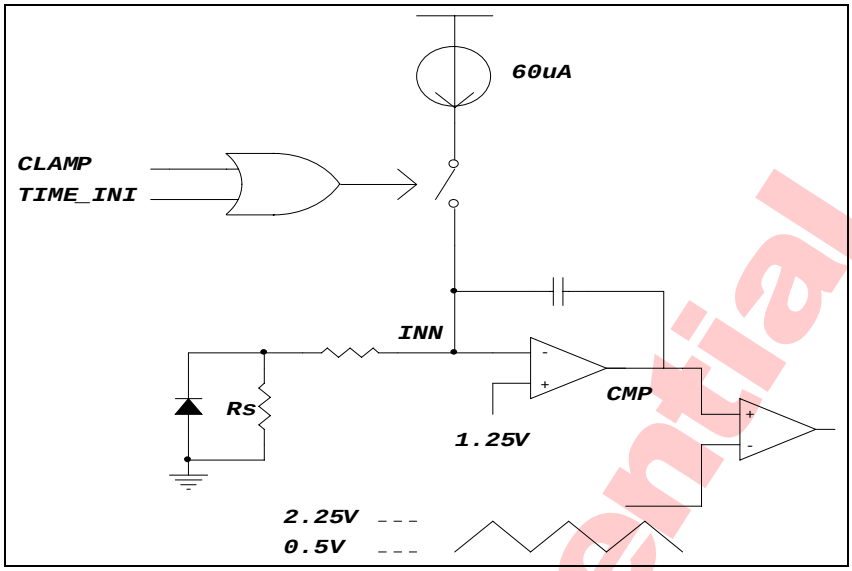

Fig. 14 The scheme of over voltage clamping

Another function of CLAMP pin is shown as Fig. 15. When voltage level of ISEN pin is higher than 2.5V then NOUT has PWM output and CLAMP level is higher than 2V (e. g. 2.5V). BIT3193 will shut down its output after counting 14 cycles based on CTOSC frequency.

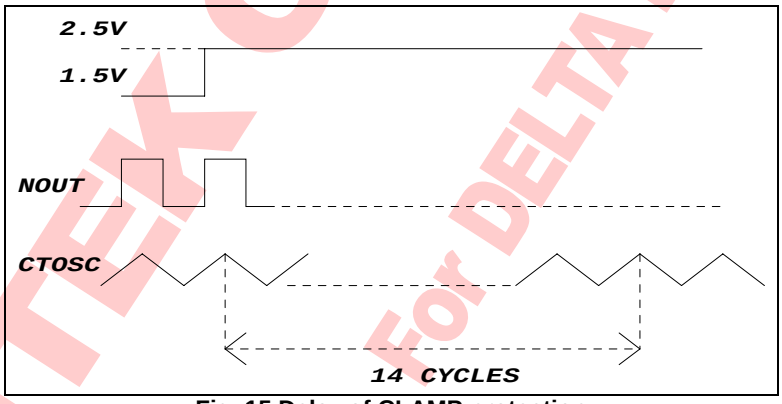

Fig. 15 Delay of CLAMP protection

2.9. Output driving circuit

NOUT of BIT3193 is controlled by PWMOUT, protection circuit and ON/OFF associated by an AND gate, shown as Fig. 16. The output PWM signal level is IC_VDD and ground by its output driving MOSFET circuit.

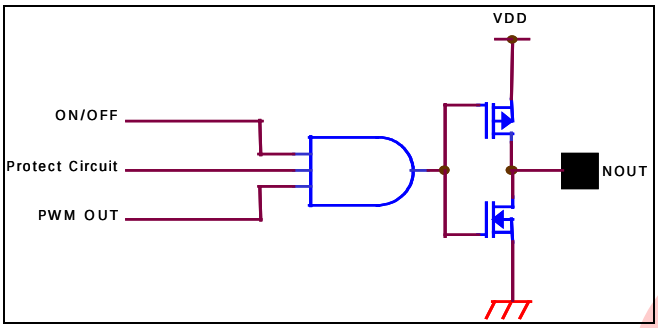

Fig. 16 BIT3193 NOUT output driver

3. Referenced external circuit design

There will be some referenced external circuit designs for BIT3193 in following sections. They are recommended and matched to the characteristics of BIT3193.

The working voltage range of BIT3193 is 4.5V~8V and recommended operation voltage is 6.5V. When the input voltage is lowed than the UVLO voltage (3.8V) of BIT3193, it will be shut down. When input voltage of BIT3193 is higher than UVLO (4V) and the input of ON/OFF pin is higher than 1V, then BIT3193 will be turned on.

Fig. 17 is a fixed input voltage design, like a LDO, to supply stable voltage to BIT3193 when the system input voltage is fluctuant. This regulator circuit needs to be designed carefully to supply enough input voltage to BIT3193, also the power rating of R2 and D1 need to be considered when they operate at maximum input voltage. The capacitor C3 used in this voltage regulator should be large enough to avoid high voltage ripple occurred in BIT3193 VDD pin.

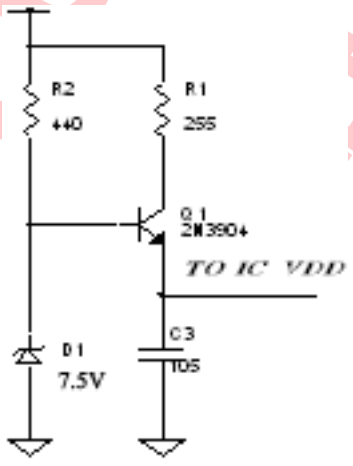

Fig. 17 IC_VDD power circuit

3.1. Feedback scheme

The current sensing and feedback control circuit is shown as Fig. 18that the load is operated at

alternative current.

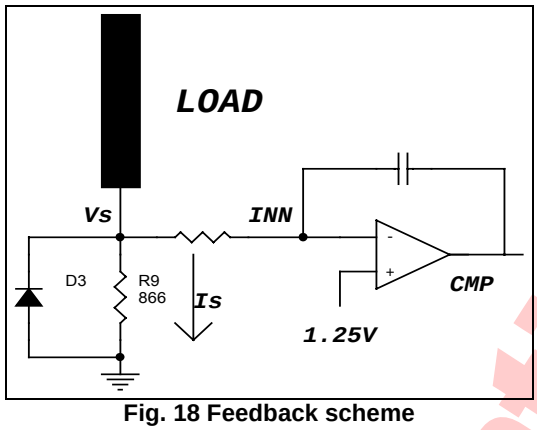

Fig. 18 Feedback scheme

The load current can be learned as following equation:

$$I_s = \frac{V_s}{R9}$$

$$V_s = \left(\frac{1.25V + \frac{VD}{2}}{\sqrt{2}} \right) \times \pi$$

When R9 is 866 Ω, the lamp current is about 4.1mA

3.2. ISEN protection circuit

ISEN pin is used as an alternative current detection circuit by connecting a resistor (R9) and a diode (D3), shown as Fig. 7. In this circuit, R8, R10 and C8 are a low-pass filter worked for filtering the ripple voltage of ISEN pin when there is a normal operation alternative current. When open-load is happened, ISEN pin voltage is lower than 1.3V, and TIMER pin is higher than 2.5V after CTPWM counts over 32 cycles, then BIT3193 assumes it is operated under open-load condition and shut down itself.

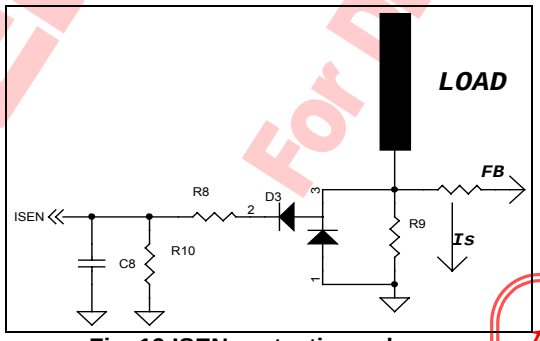

Fig. 19 ISEN protection scheme

3.3. CLAMP protection circuit

CLAMP used as the over voltage protection function that can avoid the transformer provides an unexpected high voltage to damage itself. The referenced alternative voltage clamping circuit is shown as Fig. 20. The

transformer output voltage is divided by capacitors C2 and C3 then feeds to CLAMP pin by a rectifier diode D2.

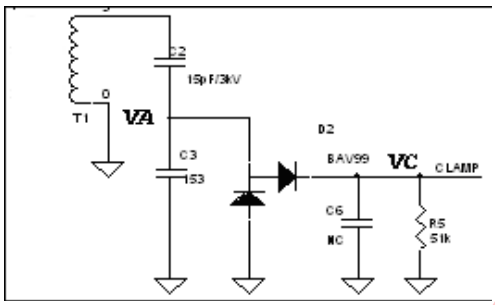

Fig. 20 Clamp circuit scheme

The clamped voltage is calculated by following equations.

$$VA_{(P-P)} = VC \times 2VD$$

$$V_{CLAMP(P-P)} = VA_{(P-P)} \times \frac{X_{C2} + X_{C3}}{X_{C3}}$$